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FEE TRANSMITTAL

Patent fees are subject to annual revision on October 1

These are the fees effective October 1, 1997

Small Entity payments must be supported by a small entity statement,

otherwise large entity fees must be paid See Forms PTO/SB/09-12

Express Mailing Label No.: **EL547741975****Complete If Known**

Application Number	
Filing Date	November 15, 2000
First Named Inventor	Domingo G. Garcia
Examiner Name	
Group / Art Unit	
Attorney Docket No.	TI-28900

TOTAL AMOUNT OF PAYMENT (\$ 790.00)**METHOD OF PAYMENT**

- 1.
- ☒
- The Commissioner is hereby authorized to charge to the following Deposit Account,

Deposit Account Number

20-0668

Deposit Account Name

Texas Instruments Incorporated

- ☒
- Charge any additional fee required or credit any overpayment
- ☐
- Charge all indicated fees and any additional fee required or credit any overpayment

- 2.
- ☐
- Payment Enclosed:**

☐ Check
 ☐ Money Order
 ☐ Other
FEE CALCULATION**1. BASIC FILING FEE**

Large Fee Code	Entity Fee (\$)	Small Fee Code	Entity Fee (\$)	Fee Description	Fee Paid
101	710	201	395	Utility filing fee	\$ 710
106	310	206	165	Design filing fee	\$
107	480	207	270	Plant filing fee	\$
108	760	208	395	Reissue filing fee	\$
114	150	214	75	Provisional filing fee	\$
SUBTOTAL (1)					(\$ 710)

2. EXTRA CLAIM FEES

Total Claims	Extra Claims	Fee from below	Fee Paid
10	-20**= 0	18	0
Independent Claims	4	-3**= 1	80
Multiple Dependent		260	

**or number previously paid, if greater; For Reissue, see below

Large Fee Code	Entity Fee (\$)	Small Fee Code	Entity Fee (\$)	Fee Description
103	18	203	11	Claims in excess of 20
102	78	202	41	Independent Claims in excess of 3
104	260	204	135	Multiple dependent claims in excess of 3
109	78	209	41	**Reissue independent claims over original patent
110	18	210	11	**Reissue claims in excess of 20 and over original patent
SUBTOTAL (2)				(\$ 80)

FEE CALCULATION (continued)**3. ADDITIONAL FEES**

Large Fee Code	Entity Fee (\$)	Small Fee Code	Entity Fee (\$)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	380	216	200	Extension of time within second month	
117	870	217	475	Extension of time within third month	
118	1,360	218	755	Extension of time within fourth month	
128	1,850	228	1,030	Extension of time within fifth month	
119	300	219	155	Notice of Appeal	
120	300	220	155	Filing a brief in support of an appeal	
121	260	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,210	241	660	Petition to revive - unintentional	
142	1,210	242	660	Utility issue fee (or reissue)	
143	430	243	225	Design issue fee	
144	580	244	335	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt.	
581	40	581	40	Recording each patent assignment per properly (time number of properties)	
146	760	246	395	Filing a submission after final rejection (37 CFR 1.129(a))	
149	760	249	395	For each additional invention to be examined (37 CFR 1.129(b))	

Other fee (specify)

Other fee (specify)

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3)**SUBMITTED BY**

Typed or Printed Name

Robert D. Marshall, Jr.

Signature

Robert D. Marshall, Jr.

Date

November 15, 2000

Complete (if applicable)

Reg Number

28,527

Deposit Account User ID

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

TI-28900

Domingo G. Garcia

Serial No:

Filed: November 15, 2000


For: Timing Recovery Device and Method for Telecommunications Systems

PRELIMINARY AMENDMENT

Ass't Commissioner for Patents
Washington, DC 20231

Dear Sir:

EXPRESS MAILING" Mailing Label No. EL547741975. Date of Deposit: **November 15, 2000**. I hereby certify that this paper is being deposited with the U.S. Postal Service Express Mail Post Office to Addressee Service under 37 CFR 1.10 on the date shown above and is addressed to: Ass't Commissioner for Patents, Washington, D.C. 20231.


Robin E. Barnum

Please amend the specification by inserting before the first line, the following sentence:

--This application claims priority under 35 USC §119(e)(1) of Provisional Application Number 60/171,346, filed December 21, 1999.--

Respectfully submitted,



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TI -28900 - 032350.B042

TIMING RECOVERY METHOD AND DEVICE FOR TELECOMMUNICATIONS SYSTEMS

* * * * *

TECHNICAL FIELD OF THE INVENTION

This invention relates generally to the field of telecommunications and is more specifically related to CAP/QAM modems and improvements therein.

BACKGROUND OF THE INVENTION

In recent years, the data rates at which communications may be carried out over conventional telephone networks and wiring has greatly increased. These increases are due, in large part, to newly adopted techniques of multiplexing and modulating signals representative of the messages or data being communicated, resulting in greatly improved communication bandwidth. In addition, the carrier frequencies at which such communications are being carried out have also increased in recent years, further improving the bit rate.

In general, the local oscillator frequencies used in a transmitting modem and a receiving modem are not identical. The frequencies of their clocks can be off by as much as 100 ppm. One of the tasks of the receiving modem is to generate a signal that allows it to sample the output of the receiver portion of the modem at the best timing instant. The best timing instant gives the best estimate of the instant to sample the transmitted data. In doing so, the receiver must first acquire and then track the frequency drift of the transmitter's clock. This invention provides a novel method for solving this problem, and is especially useful in burst CAP/QAM modems.

Use of quadrature modulation is intended to increase the information-carrying capacity of a modulated signal. One such modulation is Quadrature Amplitude Modulation (QAM), described by Betts et al. in U.S. Patent No. 5,859,877. QAM involves

transmitting data as a sequence of two-dimensional complex signals, i.e. with both in-phase and quadrature components. Each symbol, is assigned a specific pre-defined value according to the data it represents. A set of all of the values available for transmission is termed a constellation, and so resembles a constellation when graphically plotted on a two-dimensional basis.

Another modulation scheme is Carrierless Amplitude Phase modulation (CAP). Receivers using CAP modulation are a bandwidth-efficient means for receiving modulated signals using two-dimensional pass band line code in which the symbol data is organized in I and Q pairs. Knutson et al, U.S. Patent No. 5930,309, describes a receiver signal processing system for CAP signals. The I and Q data in such a system are filtered with orthogonal I and Q band pass filters having a common pass band. With CAP, processing is done in the pass band of the filters, which eliminates the need for a carrier tracking loop. However, tighter symbol timing constraints is required due to the frequencies of the pulses transmitted. CAP signals can resemble QAM signals except the transmitted data is not spinning or rotating at a carrier frequency.

There are several conventional ways to perform timing recovery in a CAP/QAM system. One method is to implement a phase lock loop (PLL) using a combination of analog and digital techniques as shown in Figure 1. A Timing Phase Detector (TPD)

101 processes the incoming data samples, $s[n]$, sampled from a signal $S(t)$ by using an analog to digital converter (A/D) 104. One known method, which can perform the function of the TPD 101, is a Band Edge Component Maximization (BECM) process which generates an error signal that is proportional to the difference in phase between the transmitter and receiver clocks. The error signal generated by the TPD 101 is filtered (or averaged) and passed on to a digital to analog (D/A) converter 102. The D/A converter output is used to control the frequency of a voltage controlled oscillator (VCO) 103. The advantage of this approach is that the rest of the receiver does not need to comprehend the timing mismatches. It assumes that the incoming data stream has been sampled at the optimum instant. However, a disadvantage of this approach is the mixing of both analog and digital circuitry.

Another known method for performing timing recovery is an all digital implementation of a PLL as illustrated in Figure 2. The receiver A/D converter is clocked by a free running oscillator 201. As in the first method, a Timing Phase Detector 101 is used to determine the phase error between the transmitter and receiver clocks according to the frequency of the free running oscillator 201. The error signal from the TPD 101 is then passed to an interpolator 202. The interpolator 202 generates optimally sampled data samples $s^*[n]$ based on the signal $S(t)$ sampled by the free running oscillator at a frequency regulated by the receiver clock. The interpolator 202 adds a

fractional delay (less than 1 sample period delay) between the A/D converter and the rest of the receiver processing based on the error signal. The amount of delay is increased or decreased to correct for the transmitter clock drift measured by the TPD. A disadvantage of this method arises when a sample is to be inserted or deleted and the amount of delay required by the interpolator is more than one sample period to be inserted and less than one sample period to be deleted, respectively. As a consequence, when a sample must be inserted, for example the receiver has one sample period less time to process the signal and information may be lost.

SUMMARY OF THE INVENTION

Accordingly, a need has arisen in the art for a method and apparatus to provide timing recovery for CAP/QAM modems whereby the highest valued coefficients or tap weights of the system equalizers remain substantially centered in a tracking buffer, thereby preventing these coefficients from drifting to one side of the filter.

In accordance with the present invention, a timing recovery method and device are provided for processing a digital signal having an in-phase portion and a quadrature portion. An in-phase equalizer may be provided for processing an in-phase portion of the signal, and a quadrature equalizer may be provided for processing the quadrature portion of the signal.

A buffer management device is provided for storing a set of in-phase coefficients and a set of quadrature coefficients in a memory device such as tracking buffers. The in-phase and quadrature coefficients are used to define the characteristic functions of the in-phase and quadrature equalizers. The buffer management device compares the relative movement of the largest coefficients within the tracking buffers and shifts the in-phase and quadrature coefficients within the tracking buffer such that the largest in-phase and quadrature coefficients remain substantially centered within the tracking buffer. Thus, as the coefficients are updated to correct for timing drift, the buffer

management device prevents the largest coefficients from migrating out of the tracking buffer.

Other technical advantages of the present invention will be readily apparent to one skilled in the art from the following figures, descriptions, and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and its advantages thereof, reference is now made to the following description taken in conjunction with the accompanying drawing, wherein like reference numerals represent like parts, in which:

FIGURE 1 is a block diagram of a prior art Phase Lock Loop;

FIGURE 2 is a block diagram of a prior art digitally implemented Phase Lock Loop;

FIGURE 3 is a block diagram of one embodiment of a timing recovery device for a CAP/QAM receiver according to the invention;

FIGURE 4 is an example of a length-32 set of coefficient values in a filter buffer for a converged equalizer;

FIGURE 5 is an example of a length-32 set of coefficient values in a filter buffer reflecting timing drift for an equalizer after a period of time;

FIGURE 6 is diagram of a length-32 tap digital filter for a timing recovery device according to the invention; and

FIGURE 7a and 7b are diagrams of a length-32 tap digital filter for a timing recovery device illustrating the limits of a system using length-32 filter buffers within 128-element tracking buffers.

DETAILED DESCRIPTION OF THE INVENTION

The proposed invention involves a modified CAP/QAM device for receiving and processing a signal. An embodiment of the receiver 300 according to the invention is illustrated in Figure 3. The receiver 300 can be implemented solely through hard-coded electronics or can utilize a computer and software for the digital signal processing.

In a receiver 300 according to the invention, an analog signal $s(t)$ can be digitized by an analog to digital (A/D) converter 301. The A/D converter can be incorporated into the receiver or can be implemented separately.

The processing of the digitized signal begins with two phase splitting filters implemented as linear adaptive fractionally spaced equalizers. A linear adaptive equalizer is simply a Finite Impulse Response (FIR) Filter with programmable filter coefficients. A fractionally spaced equalizer processes more than 1 A/D sample per QAM/CAP symbol period.

A FIR filter implements the difference equation

$$y(n) = \sum_{k=0}^{N-1} w[k]x[n-k],$$

where $x[n]$ are the input samples, $y(n)$ is the filtered output, and $w[k]$ are the coefficients (also known as tap weights). In the QAM/CAP receiver, the equalizers comprise an in-phase equalizer 302 and a quadrature equalizer 303, which are implemented as

$$I(n) = y(n) = \sum_{k=0}^{N-1} w[k]x[n-k] \text{ and}$$

$$Q(n) = y(n) = \sum_{k=0}^{N-1} w_Q[k]x[n-k],$$

where $x[n]$ are the input samples from the A/D converter 301 and $w_I[k]$ are the coefficients of the in-phase equalizer 302 and $w_Q[k]$ are the coefficients of the quadrature equalizer 303, and $I(n)$ and $Q(n)$ are the outputs of the in-phase equalizer 302, and quadrature equalizer 303, respectively. The coefficients for the two filters, which can be stored in a buffer management device 304 or in a separate memory device or buffers, define the impulse response of the equalizers. There is one set of coefficients for the in-phase equalizer and one set of coefficients for the quadrature equalizer. The length of the equalizer filters (N in the above equations) can be set according to system parameters such as the particular characteristics of the channel being equalized.

During the start up state of the receiver, the two equalizers are trained using a standard Least Means Square (LMS) algorithm using a known training sequence. Training an equalizer refers to the changing of the coefficients over some time period such that a criterion is satisfied. In this case, the minimization of the mean square error is the criterion. The LMS algorithm iteratively updates the filter coefficients using the following equations:

$$e(n) = d(n) - \mathbf{w}^H(n)\mathbf{u}(n), \text{ and}$$

$$\mathbf{w}(n+1) = \mathbf{w}(n) + \mu \mathbf{u}(n)e^*(n),$$

where $e^*(n)$ is the complex conjugate of the estimation error, $w(n)$ is the tap weight vector (i.e. the set of coefficients), $w(n+1)$ is the updated coefficient set after one iteration, $d(n)$ is the desired result, and $w^H(n)u(n)$ is the output of the equalizer filter, and μ is the update step size ($0 < \mu < 1$). The superscript H denotes the Hermitian transposition (i.e. the operation of vector transposition with complex conjugation). Each equalizer has its own set of coefficients which can be stored in separate buffers and which are updated separately.

The desired results $d(n)$ are points of a QAM constellation. For a simple 4-QAM constellation, the two dimensional coordinates, (x,y) , are $(1,1)$, $(-1,1)$, $(-1,-1)$, and $(1,-1)$. The desired results are then a sequence of 1's and -1's. During training, $d(n)$ can be a sequence that is known to both the transmitter and receiver. In the QAM/CAP receiver being described, the two equalizers are trained and updated independently. The in-phase equalizer uses the x coordinate values as the desired results while the quadrature equalizer uses the y coordinate values as desired results. In the above equations, $u(n)$ for the in-phase equalizer is represented as $I(n)$, and $u(n)$ for the quadrature equalizer is represented as $Q(n)$. After a number of iterations, the estimation error should converge to some minimum value and the coefficients for the equalizers should converge to steady state values. An example of

a converged equalizer with a set of 32 coefficients is shown in Figure 4.

For updating the coefficients after training, the desired results $d(n)$ are obtained from the outputs of the slicer 305. The slicer 305 selects the closest constellation point to the equalizer outputs.

Thus, in the 4-QAM example, if $I(n)$ (the output of the in-phase equalizer) is 0.75, then the closest x coordinate, the sliced value, is 1 (0.75 is closest to 1 rather than -1). Therefore, the sliced value, $I'(n) = 1$, is the $d(n)$ to be used in the error equation. The error $e(n)$ would then be

$$\begin{aligned} e(n) &= d(n) - \mathbf{w}^H(n)\mathbf{u}(n) \\ &= I'(n) - I(n) \\ &= 1 - 0.75 \\ &= 0.25 \end{aligned}$$

where $I'(n)$ is the value of the slicer output and $I(n)$ is the equalizer output.

In conventional QAM/CAP receivers, the adaptive equalizer is used to compensate for changes in channel characteristics. A previously stated, timing recovery is performed by a separate timing recovery block. However, because a fractionally spaced equalizer has the ability to incorporate a fractional delay into its impulse response, the adaptive

fractionally space equalizer can be used as the timing recovery block as well as the channel compensation block.

Assuming that the transmission channel has no time varying aspect to it, the transmitter and receiver clocks can drift apart, thereby creating a timing drift. To correct for timing drift, the adaptive equalizers can be continually updated using the LMS algorithm. The coefficients of the equalizers will change such that the mean square error $e(n)$ is continuously minimized. This LMS algorithm tracks the timing drift.

After some time, the equalizer coefficients may look like those in Figure 5. The highest valued coefficients have drifted to one side of the filter. Before the invention, the coefficients with the most energy could drift out of a buffer storing the coefficients, causing the receiver to fail.

To overcome this problem, the present invention provides a buffer management device 301 having an equalizer filter 601 designed to monitor the movement of the coefficients within a tracking buffer 604. An example of a length-32 tap digital filter according to the invention is illustrated in Figure 6. At time $t(0)$, the data filter buffer 602 and the coefficient filter buffer 603, each of length 32, are used to compute the filter output. The data filter buffer 602 and the coefficient filter buffer 603 can be centered inside the much longer buffers, such as the tracking buffers 604. Alternatively,

the coefficient filter buffer 603 and the data filter buffer 602 can be separate buffers which point to the locations of the set of coefficients, represented by 603, and the set of data, represented by 602, which are to be used in the equalizer filter. In the example, the tracking buffers are of length 128. The coefficients 605 outside the 32 centered coefficients 605 are initialized to zero. As described above, the filter output of either the filters of the in-phase equalizer 302 or quadrature equalizer 303 can be represented as $y(n) = \sum_{k=0}^{N-1} w[k]x[n-k]$.

For a length-32 filter with an overall buffer length of 128, as provided in the example, the output at $t(0)$ can be represented as:

$$y[n+i] = \sum_{k=i}^{i+N-1} x(n+i)w[n+i-k],$$

where initially $i = 48$, (i.e. the first element of the length-32 filter buffers centered within the tracking buffers).

A buffer management device 304, which can be implemented as hard coded electronics or can utilize a computer and software, determines the direction of the movement of the coefficients 605 by comparing sets of filter coefficients 605 to determine which sets hold the greatest values. In this way the buffer management device 304 can track the direction of timing drift. Accordingly, the buffer management device 304 allows for centering of the coefficients 605 by adjusting the relative

positions of the coefficients 605 within the their respective buffers. While the methods described below for comparing and centering coefficients are directed one set of coefficients, either the I or Q coefficients may be calculated or both.

In an initial state, the coefficients 605 in the center of the coefficient filter buffer 603 normally hold the greatest values. By comparing the values of the center coefficients 605 to the coefficient values to the left of center as well as comparing the center coefficient values with the coefficient values to the right of center, the buffer management device 301 can determine which way the coefficients 605 are moving.

One scheme for tracking coefficients 605 is by comparing the sum of the absolute values of a contiguous set of highest valued coefficients 605. At least three sums may be computed based on a set of coefficients 605 about the center of the entire set of coefficients 605, a set to the left of center and a set to the right of center. Choosing the length and the relative positions of the sets used for the summations depends upon the initial characteristics of the filter, but preferably encompass most of the highest valued coefficients 605. By choosing longer sets or more than three sets, the more operations which would be required to compute the summations. Whereas by choosing shorter or fewer sets, the greater is the chance of an error in estimating drift direction. For example, the total

summation of all coefficient sets can be 80% of the total summation of all coefficients in a tracking buffer.

The sets of coefficients chosen for summation can be contiguous or overlapping. For example in Figure 4, three contiguous sets of a length-8 coefficient set encompass most of the highest valued coefficients. The following summations can represent the sums of the absolute values of the three overlapping sets of eight coefficients:

$$left_sum = \sum_{k=i+N/2-12}^{i+N/2-4} abs(w[k]),$$

$$center_sum = \sum_{k=i+N/2-4}^{i+N/2+4} abs(w[k]), \text{ and}$$

$$right_sum = \sum_{k=i+N/2+4}^{i+N/2+12} abs(w[k]).$$

Once the sums of coefficients are computed, it is possible to center the sums by comparing the sums and shifting the sums accordingly.

One variation of a buffer management device according to the invention compares the summation result of the left set with the summation result of the center set. If the summation of the left set is greater, then the device shifts the filter buffers storing the coefficient sets to the left within the tracking buffers. If the summation result of the left set is not greater, the device compares the summation result of the center set with the summation result of the right set. If the summation

of the right set is greater than the summation of the center set, then the device shifts the filter buffers to the right within the tracking buffers. If the summation of the right set is not greater, then the position of the filter buffers within the tracking buffers is not changed. While the above method describes comparing one set of coefficients, both sets of in-phase and quadrature filter coefficients can be centered together. Alternatively, both sets may be compared separately, and the amount of centering can be the average of the centering result performed on both sets of coefficients.

To center the coefficient set, the buffer management device 301 can shift the filter buffers storing the coefficients for the in-phase and quadrature equalizers by an amount, adj , sufficient to move the high valued coefficients so that they are substantially centered within the filter buffer. The amount of adjustment required depends upon the variability of drift in the system and can be adjusted accordingly. One way of automatically adjusting this amount, adj , is by using a feedback loop which compares the current coefficient summation sets with a prior set and adjusting the amount of shift, adj , accordingly. The amount of adjustment can be the distance from the center of the center sum to the closest edge of an adjacent set. In the current example, $adj = 4$.

The comparison performed by the buffer management device can be represented by the following algorithm:

If $left_sum > center_sum$, then $i = i - adj$
else if $right_sum > center_sum$, then $i = i + adj$,
else do not change i .

Thus if i has been changed, the filter is operating on 32 different data and coefficient buffer elements. As a consequence, the above device allows a receiver to track any timing drift where the filter buffers have not drifted past the edges of the tracking buffers. Figures 7a and 7b illustrate the limits of the example the system using length-32 filter buffers within 128-element tracking buffers. The time it takes for the coefficients to drift to the edge of the tracking buffers depends on the difference in the transmitter and receiver clock frequencies. The length of the tracking buffers should be chosen such that the coefficients will not reach the edges within the time frame of the transmission burst. If the tracking buffers were of infinite length, the receiver can hypothetically track the timing difference of an infinite length transmission.

The present invention is ideally suited for CAP/QAM modems that use burst messages. The length of the buffer can be made as large as required to take into account an anticipated worst case burst length as well as the expected instability in the transmitter and receiver clocks.

Although the invention has been described here by reference to specific embodiments thereof, such embodiments are

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susceptible of variation and modification without departing from the spirit and scope of the provided claims.

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WHAT IS CLAIMED IS:

1. A method for timing recovery of a digital signal in a telecommunications receiver, comprising:
 - tracking a plurality of coefficients in a tracking buffer for timing drift,
 - centering the plurality of coefficients in the tracking buffer,
 - filtering, through an equalizer, the digital signal with the plurality of coefficients, and
 - updating the plurality of coefficients in the tracking buffer.
2. A method for timing recovery of a digital signal according to claim 1, wherein:
 - the step of tracking the plurality of coefficients further comprises,
 - summing a set of left coefficients,
 - summing a set of center coefficients,
 - summing a set of right coefficients,
 - comparing the set of left coefficients, the set of center coefficients, and the set of right coefficients to obtain a set with the greatest weighting; and

the step of centering the plurality of coefficients further comprises centering the plurality of coefficients about the set with the greatest weighting.

3. A method for timing recovery of a digital signal in a telecommunications receiver, comprising:

splitting the digital signal into an in-phase input signal and a quadrature input signal,

tracking a plurality of coefficients in a tracking buffer for timing drift, wherein the coefficients are in-phase coefficients,

centering the plurality of in-phase coefficients in the tracking buffer,

centering the plurality of quadrature coefficients in the tracking buffer,

filtering, through an in-phase equalizer, the in-phase signal with the plurality of in-phase coefficients,

filtering, through a quadrature equalizer, the quadrature signal with the plurality of quadrature coefficients,

updating the plurality of in-phase coefficients in the tracking buffer, and

updating the plurality of quadrature coefficients in the tracking buffer.

4. A method for timing recovery according to claim 3, further comprising:

tracking a plurality of coefficients in a tracking buffer for timing drift, wherein the coefficients are quadrature coefficients.

5. A timing recovery device for processing a digital signal, comprising:

an equalizer for processing said digital signal,

a filter buffer for storing a plurality of equalizer coefficients to be applied to said equalizer, and

a buffer manager for tracking the equalizer coefficients within the filter buffer, and for shifting the coefficients within the filter buffer such that the coefficients remain substantially centered within the filter buffer.

6. A timing recovery device according to claim 5, wherein the tracking buffer further comprises:

a data tracking buffer for storing a portion of said signal, and

a coefficient tracking buffer for storing said equalizer coefficients.

7. A timing recovery device according to claim 5, further comprising:

a data tracking buffer for pointing to said portion of said signal stored in said tracking buffer, and

a coefficient tracking buffer for pointing to said equalizer coefficients.

8. A timing recovery device for processing a digital signal having an in-phase portion and a quadrature portion, comprising:

an in-phase equalizer for processing said in-phase portion of said signal;

an in-phase tracking buffer for storing a plurality of in-phase equalizer coefficients to be applied to said in-phase equalizer;

a quadrature equalizer for processing said quadrature portion of said signal;

a quadrature tracking buffer for storing a plurality of quadrature equalizer coefficients to be applied to said quadrature equalizer; and

a buffer manager.

9. A timing recovery device according to claim 8, wherein:

the buffer manager is designed for tracking the in-phase equalizer coefficients within the in-phase tracking buffer, for shifting the in-phase coefficients within the in-phase tracking buffer such that the in-phase coefficients remain substantially centered within the in-phase tracking buffer, and for shifting

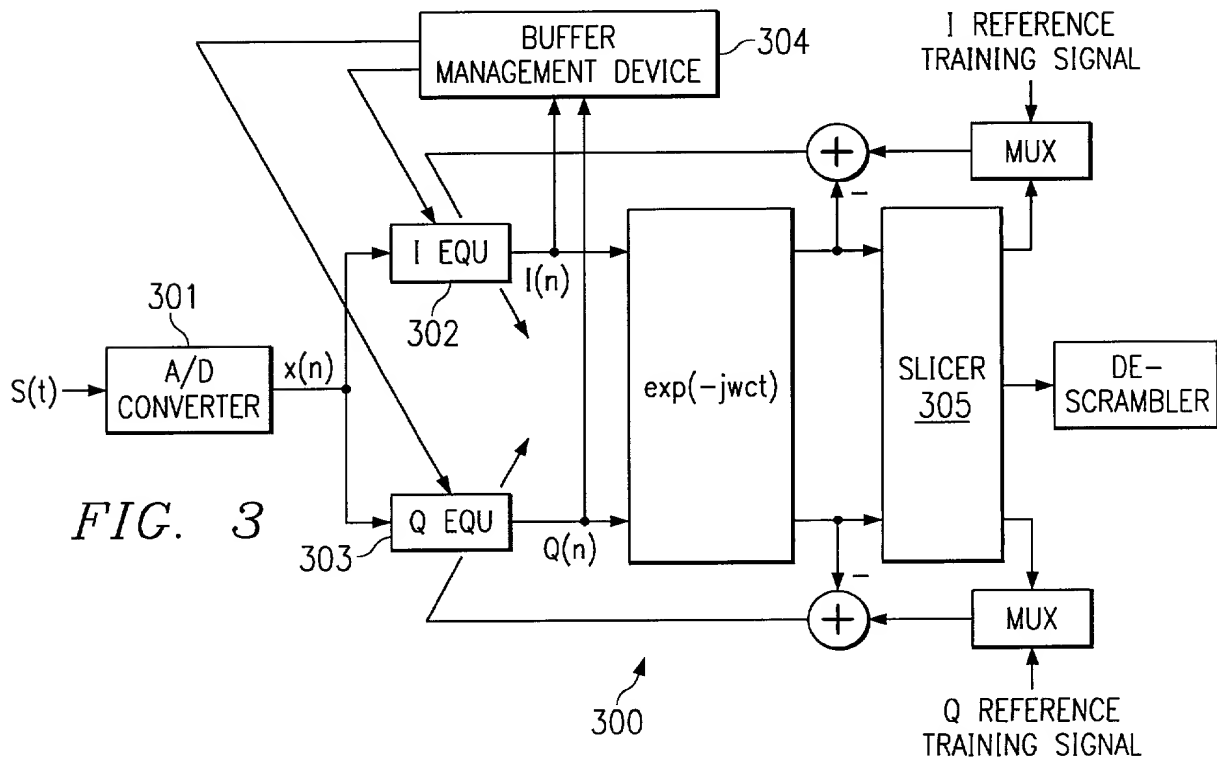
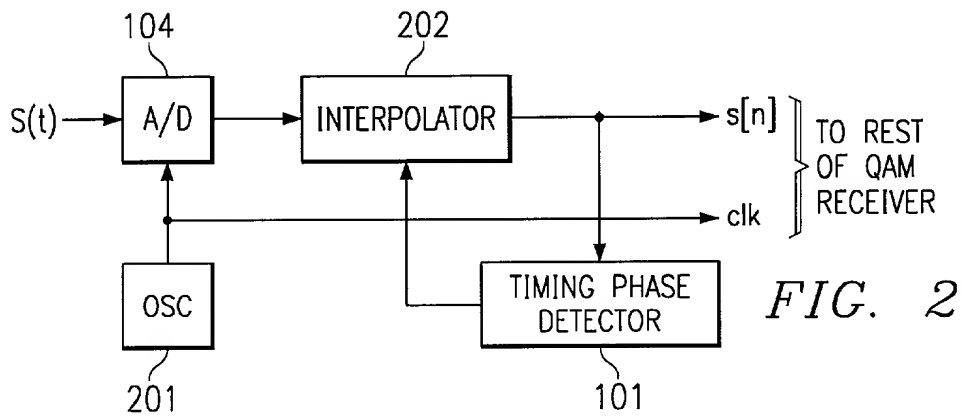
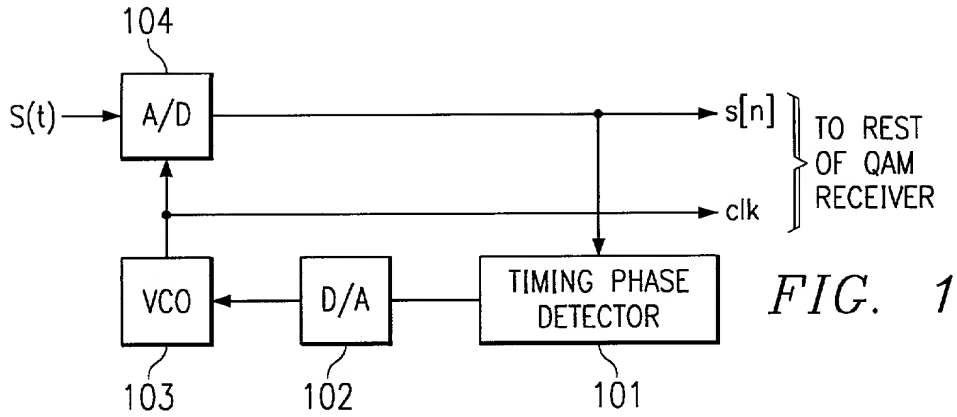
the quadrature coefficients within the quadrature tracking buffer such that the quadrature coefficients remain substantially centered within the quadrature tracking buffer.

10. A timing recovery device according to claim 8, wherein:

the buffer manager is designed for tracking the quadrature equalizer coefficients within the quadrature tracking buffer, for shifting the in-phase coefficients within the in-phase tracking buffer such that the in-phase coefficients remain substantially centered within the in-phase tracking buffer, and for shifting the quadrature coefficients within the quadrature tracking buffer such that the quadrature coefficients remain substantially centered within the quadrature tracking buffer.

ABSTRACT OF THE DISCLOSURE

A timing recovery device for CAP/QAM modems includes an equalizer filter designed to monitor the movement of the filter coefficients within a memory buffer and to adjust the relative position of the filter coefficients within the memory buffer so that the coefficients remain substantially centered within the buffer.



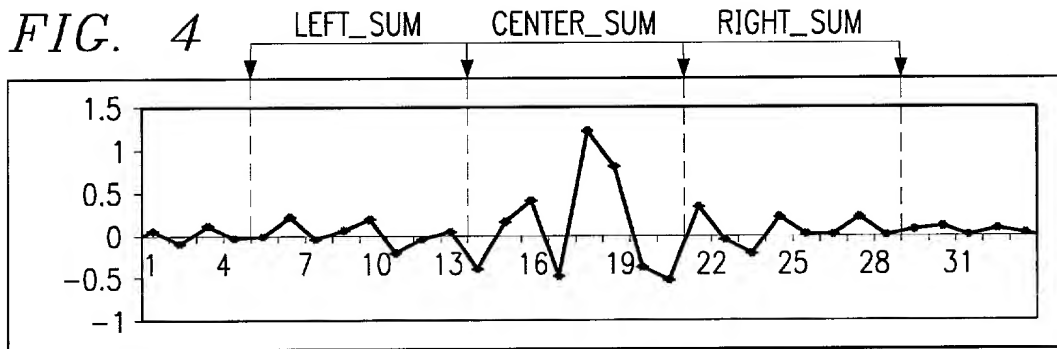
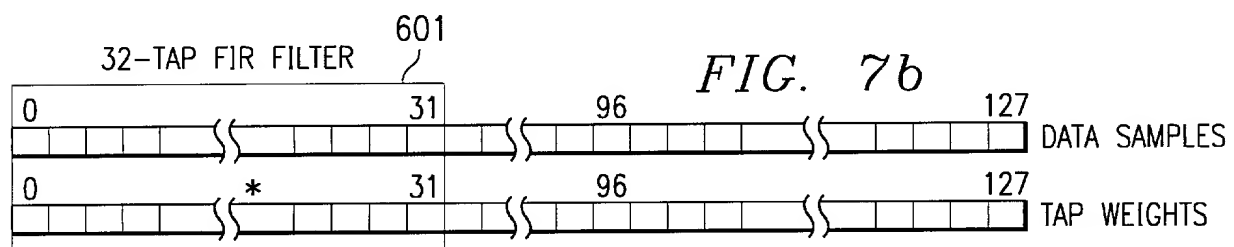
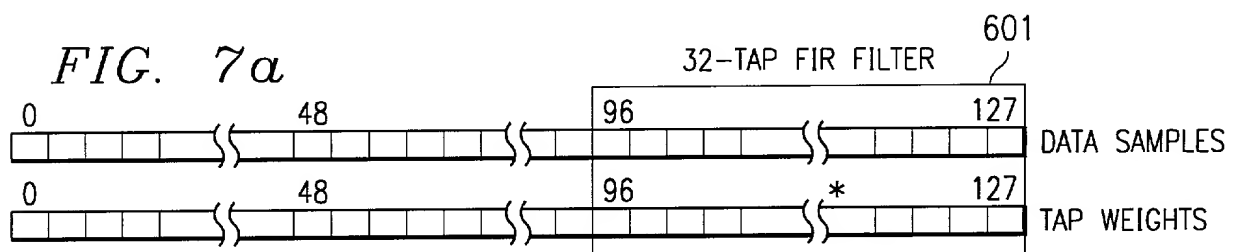
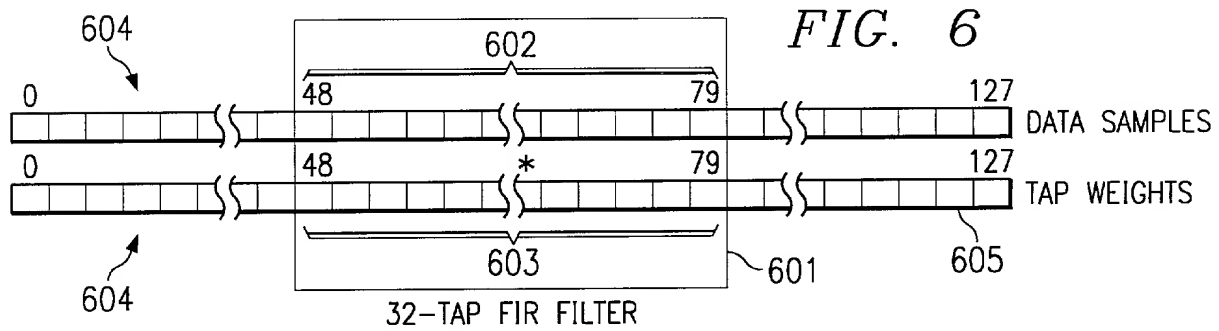
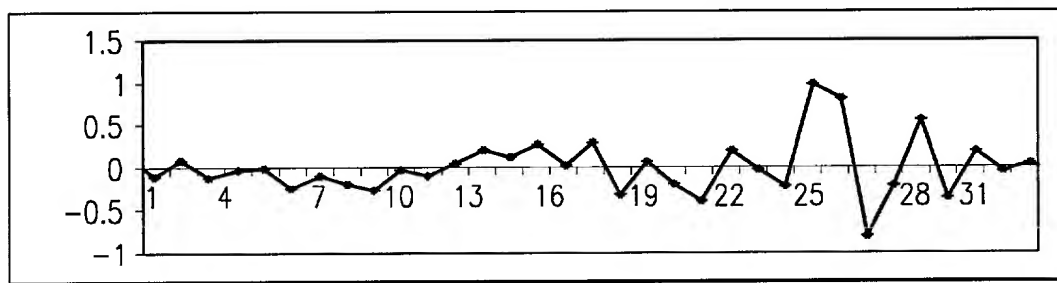


FIG. 5



APPLICATION FOR UNITED STATES PATENT

Declaration and Power of Attorney

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name; that I believe that I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought, on the invention entitled as set forth below, which is described in the attached specification; that I have reviewed and understand the contents of such specification, including the claims, as amended by any amendment specifically referred to in the oath or declaration; that no application for patent or inventor's certificate on this invention has been filed by me or my legal representatives or assigns in any country foreign to the United States of America; and that I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in 37 C.F.R. § 1.56.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

TITLE OF INVENTION:

TIMING RECOVERY METHOD AND DEVICE FOR TELECOMMUNICATIONS SYSTEMS

I hereby appoint the following attorneys to prosecute this application and transact all business in the Patent and Trademark Office connected therewith:

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12/15/99